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EXAMINER	
NGUYEN, TUNG X	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,902	GILBERT, BARRIE	
	Examin r	Art Unit	
	Tung X Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 2/20/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-9,13-18,21 and 24* is/are allowed.

6)☒ Claim(s) *2-5,10-12,19,20,22,23 and 25-31* is/are rejected.

7)☒ Claim(s) *28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2-5, 22-23, 25-27, 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita et al. (u.s.p 4,906,836).

As to claims 2-5, 22-23, 25-27, 30 Yamashita et al. disclose in Fig. 1, a measurement system comprising: a first log amp (LOG1) having a current output (inherent); a second log amp (LOG2) having a current output (inherent); and coupling to a differencing circuit (AMP1), wherein the differencing circuit is arranged to continuously process output from the first (LOG1) and second (LOG2) log amps; and the differencing circuit (AMP1) having a summing node (at the negative node and the positive node of AMP1, for example the feed back loop R2 and R1 meet at the negative node). According to Applicant's remark on page 7 filed on 02/20/04, Logarithmic Amplifiers are progressive compression log amps. Therefore, the log amps (log1 & log2 of figure 1) of Yamashita et al. are progressive compression log amps.

As to claim 29, Yamashita et al. disclose in Fig. 1, the adding limitation of the Log Amp have current-mode outputs be considered as the difference voltage signals between the negative node and positive node of the amplifier (AMP1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10-12,19-20, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. (u.s.p 4,906,836).

As to claims 10-12, 19-20, 31, Yamashita et al. disclose in Fig. 1, the system comprising: a first log amp (LOG 1), and the second log amp (LOG 2) arranging symmetrically about a center line (see Examiner's label on Fig. 1); and wherein the first and second log amps are co-integrated on a substrate in a package. For example, (see the abstract) mentions that "An integrated circuit includes an operational amplifier...the output of the second logarithmic amplifier is connected to the inverting input terminal of the operational amplifier", thus obviously suggesting the first and second log amps are co-integrated on the semiconductor. In regard to claimed "co-integrated on the substrate" it is note that the reference is silent such feature; However, It would have been obvious to a person having ordinary skill in the art at the time the invention that any conventional semiconductor structure could have an co-integrated on the substrate implemented as an inherent design variations, as also well-known in the existing semiconductor technology.

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. (u.s.p 4,906,836), in view of Belcher (u.s.p 5,789,927).

As to claim 28, Yamashita et al. disclose in Fig. 1 all limitations except for the power amplifier having an input coupled to an input of the first log amp and an output coupled to an input of the second log amp. However, Belcher disclose in Fig. 3, the power amplifier (10) having an input coupled to the first hard limiter (21) being considered as the first Log amp, and the output coupled to the second hard limiter (31) being considered as the second Log amp for measuring the error between two signals of the input and output of the power amplifier (10). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Yamashita et al., and provide the power amplifier (10), as taught by Belcher for measuring the error between two signals of the input and output of the power amplifier (10).

7. The method is considered inherent in the structure.

Allowable Subject Matter

8. Claims 6-9, 13-18, 21, and 24 are allowed.

Claim 28 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is an examiner's statement of reasons for allowance:

As to claims 6-9, 16-18, 21, and 24 the prior art does not disclose *the phase detector core coupled to the first and second log amps.*

As to claim 13, the prior art does not disclose *the first and second parasitic network coupled to the first and second log amps.*

As to claims 14-15, the prior art does not disclose the one or more log amps coupled to the input of the differencing circuit.

As to claim 28, the prior art does not disclose the power amplifier having an input coupled to an input of the first log amp and an output coupled to an input of the second log amp.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee.. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

10. Applicant's arguments filed 02/20/04 have been fully considered but they are not persuasive following the reasons:

As to claims 2, 10, 19, 20, 22, 30, 31, in re page 7, Applicant argues that Yamashita only discloses log amps, Yamashita does not disclose the Log amps are progressive compression log amps.

In response, as to claims 2, 2, 10, 19, 20, 22, 30, 31 according to Applicant's remark on page 7 filed on 02/20/04, Logarithmic Amplifiers are progressive compression log amps. Therefore, the log amps (log1 & log2 of figure 1) of Yamashita et al. are progressive compression log amps.

As to claim 4, in re pages 7-8, Applicant argues that Yamashita's differencing circuit does not have a summing node.

In response, as to claim 4, Yamashita et al.'s differencing circuit (AMP1 of figure 1) clearly disclose the summing node (at the negative/positive node of figure 1; e.g. The current flowing in the R1, and feedback's current flowing R2 and these current flow at negative node; however, the current flowing into R3, and the current flowing into R4 flow at the positive node).

As to claim 11, applicant argues that the log amps are not arranged symmetrically about a center line, because Yamashita does not disclose the physical configuration of the log amps on the substrate. Applicant states that figure 1 is merely a schematic of the circuit and not an actual layout; therefore, examiner's label in figure 1 is irrelevant.

In response, as to claim 11, the examiner points out that the claim says, "arranged symmetrically about *a* center line." The claim does not state what the center line is. Therefore, irrespective of how the log amps are arranged on the substrate, there is always some center line from which each log amp is equidistant (that is, is symmetric about). Examiner was merely showing one example of how such a line could be defined by showing the label in figure 1. Namely, if the center line is defined as the line in the middle of the two log amps, then, the log amps will necessarily be equidistance from it.

Furthermore, since applicant has not defined the type of symmetry, any two log amps located on a substrate would always be symmetric about the line in the middle of both of them.

As to claim 25, in re page 8, Applicant argues that Yamashita does not disclose the use of a reference signal as an input to either of LOG1 and LOG2.

In response, as to claim 25, Yamashita et al. clearly show in Figs. 1-4, the LOG2 using the reference node (at positive node of LOG2 of figure 1 connects to ground). Therefore, Yamashita et al. disclose the using of a reference signal at positive node of LOG2 (figure 1).

As to claim 26, in re page 8, Applicant argues that Yamashita does not identify any input signals that have the same waveform.

In response, as to claim 26, Yamashita et al. show in Fig. 2, the input signals input into the LOG/R and LOG/G with the same input signal at positive nodes of LOG/R and LOG/G. Therefore, Yamashita et al. disclose the inputs that have the same waveform.

As to claims 27, 29, in re page 8, Applicant argues that Yamashita does not disclose utilizing a modulated signal for the first and second signals, and the log amps have current-mode outputs.

In response, as to claims 27, 29, the examiner respectfully disagrees with Applicant about the issue for the following reasons: Any signals input to the Log amps (Log 1, and Log 2) producing the signals with the formular e1 = $V_T Ln(I_{f1}/I_{s1})$, and e2 = $V_T Ln(I_{f2}/I_{s2})$, so the signals will vary the amplitude depended on I_{f1}, I_{f2} and the diodes D1, D2 (see col. 1, lines 25-40). Therefore, Yamashita et al. disclose utilizing a modulated signal for the first and second signals, and the log amps have current-mode output (see col. 1, lines 25-40).

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN
5/06/04

David A. Zarneke
Primary Exam
5/10/04